


FORM PTO-1449 (Rev. 2-32)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 02-957	Serial No. 10/603,388
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		Applicant: Rajamohana Hegde et al.	
		Filing Date: June 24, 2003	Group: 2631

U.S. PATENT APPLICATION DOCUMENTS

Examiner Initial	Document Number	Filing Date	Name	Class	Subclass	Publication Date if Appropriate
JAT	1.	2001/0035994	02/28/2001	Agazzi et al.		11/01/2001
JAT	2.	2001/0035997	01/17/2001	Agazzi		11/01/2001
JAT	3.	2002/0012152	07/23/2001	Agazzi et al.		01/31/2002
JAT	4.	2002/0080898	03/01/2002	Agazzi et al.		06/27/2002
JAT	5.	2002/0060827	11/20/2001	Agazzi		05/23/2002

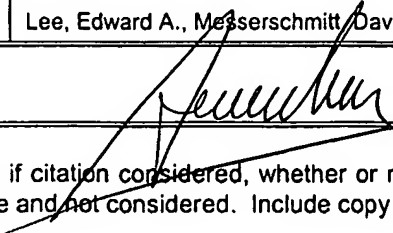
U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclasses	Filing Date if Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

JAT	6.	Lee, Edward A., Messerschmitt, David G., <i>Digital Communication-Second Edition</i> , pp. 406-409.
EXAMINER 		DATE CONSIDERED <u>3/2/2006</u>

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

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JAT	7.	Sieben, Mike, Conradi, Jan, Dodds, David E., <i>Optical Single Sideband Transmission at 10 Gb/s Using Only Electrical Dispersion Compensation</i> , Journal of Lightwave Technology, Vol. 17 No. 10, pp. 1742-1749, October 1999.
JAT	8.	Haykin, Simon S., <i>Adaptive Filter Theory</i> , pp. 8-10, 1986.
JAT	9.	Kim, Kyoung, Powers, Edward J., <i>A Digital Method of Modeling Quadratically Nonlinear Systems with a General Random Input</i> , IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 36, no. 11, pp 1758-1769, November 1988.
JAT	10.	Shanbhag, Naresh R., <i>Algorithms Transformation Techniques for Low-Power Wireless VLSI Systems Design</i> , pp. 1-36.
JAT	11.	Fettweis, Gerhard, Meyr Heinrich, <i>High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture</i> , IEEE Communications Magazine, pp. 46-55, May 1991.
JAT	12.	Parhi K. Keshab, <i>Pipelining and Parallel Processing</i> , pp. 63-64 1999. pp 63-64 & 70-73
JAT	13.	Haunstein, Sticht K., <i>Design of Near Optimum Electrical Equalizers for Optical Transmissions In the Presence of PMD</i> .
JAT	14.	Bulow, Henning, Thielecke, Tunther, <i>Electronic PMD Mitigation-From Linear Equalization to Maximum-Likelihood Detection</i> .
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JAT	15.	Boo, Montse, Arguello, Francisco, Bruguera, Javier D., Doallo Ramon, <i>High-Performance VLSI Architecture for the Viterbi Algorithm</i> , IEEE Transactions on Communications, Vol. 45, No. 2, pp. 168-176, February 1997.
JAT	16.	Fettweis, Gerhard, Meyer, Heinrich, <i>Parallel Viterbi Algorithm Implementation: Breaking the ACS-Bottleneck</i> , IEEE Transactions on Communications, Vol. 37, No. 8, pp. 785-790, August 1989.
JAT	17.	Tzou, Kou-Hu, Dunham, James G., <i>Sliding Block Decoding of Convolutional Codes</i> , IEEE Transactions on Communications, Vol. Com-29, No. 9, pp. 1401-1403, September 1981.
JAT	18.	Robertson, Patrick, Hoehner, Peter, <i>Optimal and Sub-Optimal Maximum a Posteriori Algorithms Suitable for Turbo Decoding</i> , ETT Vol. 8, pp. 119-125, March-April 1997.
JAT	19.	Black, Peter J., Meng, Teresa H., <i>A 140-Mb/s, 32-State, Radix-4 Viterbi Decoder</i> , IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, pp. 1877-1885, December 1992.
JAT	20.	Black, Peter J., Meng, Teresa H., <i>A 1-Gb/s, Four-State, Sliding Block Viterbi Decoder</i> , IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, pp. 797-805, June 1997.
JAT	21.	Fettweis, Gerhard, Meyr, Heinrich, <i>High-Rate Viterbi Processor: A Systolic Array Solution</i> , IEEE Journal on Selected Areas in Communications, Vol. 8, No. 8, pp. 1520-1534, October 1990.
JAT	22.	A. K. Yeung and J. M. Rabaey, <i>A 210Mb/s Radix-4 Bit-level Pipelined Viterbi Decoder</i> , ISSCC, 1995. pp 88-89
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JAT	23. Fettweis, Gerhard, Karabed, Razmik, Siegel, Paul H., Thapar, Hemant K., <i>Reduced-complexity Viterbi detector architectures for partial response signaling</i> , IEEE Global Telecommunications Conference, Singapore, Technical Program Conference Record, vol. 1, pp. 559-563, November 1995.
JAT	24. T.Conway, <i>Implementation of High Speed Viterbi Detectors</i> , Electronics Letters, 35(24):2089-2090, November 25 1999.
JAT	25. C. B. Shung, P. H. Siegel, G. Ungerboeck and H. K. Thapar, <i>VLSI architectures for metric normalization in the Viterbi algorithm</i> , in Proc. Int. Conf. Communications, vol. 4, Apr. 1990, pp. 1723-1728.
JAT	26. Hekstra, Andries P., <i>An Alternative to Metric Rescaling in Viterbi Decoders</i> , IEEE Transactions On Communications, Vol. 37, No. 11, pp. 1220-1222, November 1989.
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Form PTO-1449 (modified)

Atty. Docket No.
02-957Serial No.
10/603,388List of Patents and Publications for Applicant's
SUPPLEMENTAL INFORMATION DISCLOSURE
STATEMENTApplicant
Rajamohana Hegde, et al.

(Use several sheets if necessary)

Filing Date:
June 24, 2003Group:
2631U.S. Patent Documents
NoneForeign Patent Documents
NoneOther Art
See Page 1

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1						
	A2						

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						
	B2						

Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
JAT	C1	Erik Paaske and Jakob Dahl Andersen, "High Speed Viterbi Decoder Architecture", - First ESA Workshop on Tracking, Telemetry and Command Systems, ESTEC, June 1998. pp 1-8
JAT	C2	Chinnery, D. G., and Keutzer, K., "Achieving 550 MHz in an ASIC Methodology", Proceedings of the 38 th Design Automation Conference, Las Vegas, NV, Pages 420-425, June 2001. 1
JAT	C3	McGinty, Nigel C.; Kennedy, Rodney A.; and Hoeher, Peter, "Equalization of Sparse ISI Channels Using Parallel Trellises", Proceedings, GLOBECOM'98, November, 1998. pp 1-6
JAT	C4	Liu, K. J. Ray and Raghupathy, Arun, "Algorithm-Based Low-Power and High-Performance Multimedia Signal Processing", Proceedings of the IEEE, Volume 86, No. 6, June 1998.
JAT	C5	Kang, Inyup and Willson, Alan N. Jr., "Low-Power Viterbi Decoder for CDMA Mobile Terminals", IEEE Journal of Solid-State Circuits, Volume 33, No. 3, March 1998.

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INFORMATION DISCLOSURE STATEMENT — PTO-1449 (MODIFIED)

Form PTO-1449 (modified)

Atty. Docket No.

02-957

Serial No.

10/603,388

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Applicant

Rajamohana Hegde, et al.

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2631

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U.S. Patent Documents

None

Foreign Patent Documents

None

Other Art

See Page 1 and 2

Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

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JAT	C6	Furuya, Yukitsuna; Akashi, Fumio and Murakami, Shuji, "A Practical Approach Toward Maximum Likelihood Sequence Estimation for Band-Limited Nonlinear Channels", IEEE Transactions on Communications, Volume Com-31, No. 2, February, 1983.
JAT	C7	Summerfield, S., "Analysis of Convolutional Encoders and Synthesis of Rate-2/n Viterbi Decoders", IEEE Transaction on Information Theory, Volume 42, Number 4, Page 1280, July 1996. <i>pp 1-15</i>
JAT	C8	Choi, Young-bae, "A VLSI Architecture for High Speed and Variable Code Rate Viterbi Decoder" ICSPAT, Proceedings, Pages 1918-22, 2000.
JAT	C9	Reeve, J.S., "A Parallel Viterbi Decoding Algorithm", July 21, 2000.
JAT	C10	Gross, Warren J.; Gaudet, Vincent C. and Gulak, P. Glenn, "Difference Metric Soft-Output Detection: Architecture and Implementation", IEEE Transactions on Circuits and Systems II (Analog and Digital Signal Processing), Volume 48, No. 10, Pages 904-911, October 2001. <i>pp 1-8</i>
JAT	C11	Ranpara, Samirkumar, "A Low-Power Viterbi Decoder Design for Wireless Communications Applications", Int. ASIC Conference, September 1999. <i>pp 1-5</i>
JAT	C12	Boo, M.; Arguello, F.; Bruguera, J.D.; and Zapata, E.L., "High-Speed Viterbi Decoder: An Efficient Scheduling Method to Exploit the Pipelining", IEEE Int'l. August 19-21, 1996.
JAT	C13	Chinnery, David, Nikolic, Borivoje and Keutzer, Kurt, "Achieving 550 MHz in an ASIC Methodology", Presentation, Proceedings of the 38 th Design Automation Conference, Las Vegas, NV, pp. 420-425, June 2001.

PP presentation pp 1-34
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